


JC20 Rec'd PCT/PTO 04 MAR 2002

TRANSMITTAL LETTER OF THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		Attorney Docket No. 2001-1021
		U.S. Application No. 10/070172
INTERNATIONAL APPLN. NO. PCT/NL00/00613	INTERNATIONAL FILING DATE 1 SEPTEMBER 2000	PRIORITY DATE CLAIMED 2 SEPTEMBER 1999
TITLE OF INVENTION: METHOD FOR THE PRODUCTION OF A SEMICONDUCTOR DEVICE		
APPLICANT(S) FOR DE/EO/US: JAN HENDRIK BULTMAN		
Applicant herewith submits to the United States Designated Elected Office (DO/EO/US) the following items and other information:		
<ol style="list-style-type: none"> 1. <input checked="" type="checkbox"/> This is a FIRST submission of items concerning a filing under 35 U.S.C. 371. 2. <input type="checkbox"/> This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371. 3. <input checked="" type="checkbox"/> This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below. 4. <input checked="" type="checkbox"/> The US has been elected by the expiration of 19 months from the priority date (Article 31). 5. <input checked="" type="checkbox"/> A copy of the International Application as filed (35 U.S.C. 371 (c)(2)) <ol style="list-style-type: none"> a. <input checked="" type="checkbox"/> is attached hereto (required only if not communicated by the International Bureau) b. <input type="checkbox"/> has been communicated by the International Bureau. See attached PCT/IB/308. c. <input type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US). 6. <input type="checkbox"/> An English language translation of the International Application as filed (35 U.S.C. 371 (c)(2)) <ol style="list-style-type: none"> a. <input type="checkbox"/> is attached hereto. b. <input type="checkbox"/> has been previously submitted under 35 U.S.C. 154(d)(4). 7. <input type="checkbox"/> Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3)) <ol style="list-style-type: none"> a. <input type="checkbox"/> are attached hereto (required only if not communicated by the International Bureau). b. <input type="checkbox"/> have been communicated by the International Bureau. c. <input type="checkbox"/> have not been made, however, the time limit for making such amendments has NOT expired. d. <input type="checkbox"/> have not been made and will not be made. 8. <input type="checkbox"/> An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)). 9. <input type="checkbox"/> An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)). 10. <input type="checkbox"/> An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)). <p>Items 11 to 20 below concern document(s) or information included:</p> <ol style="list-style-type: none"> 11. <input checked="" type="checkbox"/> Information Disclosure Statement (IDS) w/PTO-1449 - <input type="checkbox"/> Copy of IDS citations 12. <input type="checkbox"/> Assignment Papers (cover sheet & document(s)) 13. <input checked="" type="checkbox"/> A FIRST Preliminary Amendment. 14. <input type="checkbox"/> A SECOND or SUBSEQUENT Preliminary Amendment. 15. <input type="checkbox"/> A substitute specification. 16. <input type="checkbox"/> A change of power of attorney and/or address letter. 17. <input type="checkbox"/> A computer-readable form of the sequence listing in accordance with PCT Rule 18. <input type="checkbox"/> A second copy of the published international application under 35 U.S.C. 154(d)(4). 19. <input type="checkbox"/> A second copy of the English language translation of the international application (35 U.S.C. 154(d)(4)). 20. <input checked="" type="checkbox"/> Other items or information: Application Data Sheet, Abstract on a separate sheet, International Preliminary Examination Report (PCT/IPEA/409), Article 34 claims, PCT/ISA/210 		

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U.S. APPLICATION NO. 10/070172		INTERNATIONAL APPLN. NO. PCT/NL00/00613		ATTORNEY DOCKET NO. 2001-1021	
21. <input checked="" type="checkbox"/> The following fees are submitted:				CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1)-(5):					
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<input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				+	
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SEND ALL CORRESPONDENCE TO: 745 South 23 rd Street Arlington, VA 22202 Telephone (703) 521-2297 Y&T Customer No. 000466			SIGNATURE <u>Benoit Castel</u> Benoit Castel NAME 35,041 REGISTRATION NO.		
BC/lmt Date: March 4, 2002			 00466 PATENT TRADEMARK OFFICE		

100701/10-070172

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PATENT
2001-1021

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of: Jan Hendrik BULTMAN

Appl. No.: **NEW NATIONAL PHASE
APPLICATION IN THE
UNITED STATES** Group:

Filed: March 4, 2002 Examiner:

For: METHOD FOR THE PRODUCTION OF A SEMICONDUCTOR
DEVICE

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, DC 20231

March 4, 2002

Sir:

Prior to the first Official Action and calculation of the filing fee, the following preliminary amendments and remarks are respectfully submitted in connection with the above-identified application.

IN THE ABSTRACT OF THE DISCLOSURE:

Please add the Abstract of the Disclosure attached on a separate sheet attached hereto.

IN THE CLAIMS:

Please substitute claims 1-10 as originally filed, which appear on pages 7 and 8, with claims 1-8 as filed in the Article 34 amendment of 15 November 2001. The pages containing claims 1-8 are marked "AMENDED SHEET" and are attached hereto. Following the insertion of claims 1-8, please amend the claims as follows:

Please amend the claims as follows:

--3. (amended) Method according to Claim 1 characterized in that the doping material (2) is first applied to the substrate, after which the barrier material (5, 5', 5'') is applied to the substrate on the doping material (2).--

--4. (amended) Method according to claim 1, characterized in that the diffusion barrier material (5, 5', 5'') is a dielectric material in paste form that is sintered after being applied to the substrate (1).--

--6. (amended) Method according to claim 1, characterized in that the surface resistance of the highly doped regions is between 10 and 60 ohm square and the surface resistance of the regions of low doping is between 30 and 500 ohm square.--

--8. (amended) Method according to claim 1, characterized in that an etching material is added to the diffusion material (5, 5', 5'') to etch away the substrate.--

Please add the following claim:

--9. (new) Method according to Claim 2 characterized in that the doping material (2) is first applied to the substrate, after which the barrier material (5, 5', 5'') is applied to the substrate on the doping material (2).----

REMARKS

Claim 9 has been added.

Claims 3, 4, 6, and 8 have been amended to eliminate multiple dependencies.

Docket No. 2001-1021

The substitution of claims 1-8 has been done to merely place this national phase application in into the same condition as it was during Chapter II of the International Phase.

Entry of the above amendments is earnestly solicited. An early and favorable first action on the merits is earnestly requested.

Should there be any matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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BC/lmt
Attachments

ABSTRACT OF THE DISCLOSURE

5 A method for making a semiconductor device having a
 pattern of highly doped regions (6, 6') located some distance
 apart in a semiconductor substrate (1) and regions (7, 7',
 7'') of low doping located between the highly doped regions
 (6, 6'). A diffusion barrier material (5, 5', 5'') is applied
 to the semiconductor substrate at the location of the regions
 10 of low doping by imprinting with the barrier material in the
 pattern of the regions of low doping. The doping material is
 applied after or before imprinting with barrier material so
 that the highly doped regions are formed essentially between
 the barrier material in the substrate. The doping
 15 concentrations in the regions of low doping in the highly
 doped regions can be freely adjusted independently of one
 another so that a relatively low surface resistance can be
 obtained for the highly doped regions to give good conducting
 contact with the metalisation and a high surface resistance
 20 can be achieved in the regions of low doping.

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NA. 4997 D. 9/10

PCT/NL00/00613, applicant: Stichting Energieonderzoek Centrum Nederland et al., our ref:
BO42396 Bot/MCL/cb

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Claims

(44)

- 1 Method for making a semiconductor device having a pattern of highly doped regions (6,6') located some distance apart in a semiconductor substrate (1) and regions (7, 7', 7'') of low doping located between the highly doped regions (6, 6'), wherein
 - a doping material (2) is applied to the substrate, at least in the location of the highly doped regions,
 - the substrate is subjected to a diffusion step in which atoms diffuse from the doping material into the substrate, and
 - conducting contacts (8, 8') are made above the highly doped regions,characterized in that
 - before the diffusion step a diffusion barrier material (5, 5', 5'') is applied to the substrate substantially exclusively at the location of the regions (7, 7', 7'') of low doping by imprinting with the barrier material (5, 5', 5'') in the pattern of the regions of low doping, the doping material (2) being applied in a substantially continuous layer over the substrate (1).
2. Method according to Claim 1, characterized in that the barrier material (5, 5', 5'') is first applied to the substrate (1), after which the doping material (2) is applied.
- 3 Method according to Claim 1 or 2 characterized in that the doping material (2) is first applied to the substrate, after which the barrier material (5, 5', 5'') is applied to the substrate on the doping material (2)
4. Method according to one of the preceding claims, characterized in that the diffusion barrier material (5, 5', 5'') is a dielectric material in paste form that is sintered after being applied to the substrate (1).
- 5 Method according to Claim 4, characterized in that doping material has been added to the barrier material.

AMENDED SHEET

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S. 10/10

PCT/NL00/00613, applicant: Stichting Energieonderzoek Centrum Nederland et al., our ref:
BO42396 Bot/MCL/cb

6. Method according to one of the preceding claims, characterized in that the surface resistance of the highly doped regions is between 10 and 60 ohm square and the surface resistance of the regions of low doping is between 30 and 500 ohm square.

7. Method according to Claim 6, characterized in that the concentration of the doping material in the highly doped regions is between 10^{18} cm^{-3} and 10^{21} cm^{-3} , whilst the diffusion depth is between 0.1 μm and 0.5 μm , and in that the concentration of the doping material in the regions of low doping is between 10^{17} cm^{-3} and 10^{21} cm^{-3} for a diffusion depth of between 0.1 μm and 0.5 μm .

8. Method according to one of the preceding claims, characterized in that an etching material is added to the diffusion material (5, 5', 5'') to etch away the substrate.

AMENDED SHEET

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims have been amended as follows:

--3. (amended) Method according to Claim ~~1 or 2~~ characterized in that the doping material (2) is first applied to the substrate, after which the barrier material (5, 5', 5'') is applied to the substrate on the doping material (2).--

--4. (amended) Method according to ~~one of the preceding claims,~~ claim 1, characterized in that the diffusion barrier material (5, 5', 5'') is a dielectric material in paste form that is sintered after being applied to the substrate (1).--

--6. (amended) Method according to ~~one of the preceding claims,~~ claim 1, characterized in that the surface resistance of the highly doped regions is between 10 and 60 ohm square and the surface resistance of the regions of low doping is between 30 and 500 ohm square.--

--8. (amended) Method according to ~~one of the preceding claims,~~ claim 1, characterized in that an etching material is added to the diffusion material (5, 5', 5'') to etch away the substrate.--

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Method for the production of a semiconductor device

The invention relates to a method for making a semiconductor device having a pattern of highly doped regions located some distance apart in a semiconductor substrate and regions of low doping located between the highly doped regions, wherein

- a doping material is applied to the substrate, at least in the location of the highly doped regions,
- the substrate is subjected to a diffusion step in which atoms diffuse from the doping material into the substrate, and
- 10 - conducting contacts are made above the highly doped regions.

A method for making a selective emitter in a p-type crystalline Si substrate, with which a diffusion material in the form of a doping paste, such as phosphorus paste, is applied to the substrate by screen printing is described in J. Horzel, J. Szlufcik, J. Nijs and R. Mertens, "A simple processing sequence for selective emitters", 26th PVSC, Sept. 30 -
15 Oct 3; Anaheim, CA; 1997 IEEE pp 139-142. The substrate is then dried on a conveyor belt and placed in a diffusion furnace. During the diffusion step the doping materials diffuse into the substrate whilst diffusion material moves to the regions outside the imprint of doping material via the gas atmosphere in the furnace. Relatively deep diffusion zones having a phosphorus concentration varying from 10^{20} at the surface of the substrate to 10^{17}
20 at a depth of 0.5 μm below the substrate surface are formed below the imprinted dope material. Shallow diffusion zones having a low phosphorus concentration, varying from 10^{19} at the substrate surface to 10^{18} at a depth of 0.2 μm , are formed outside the region of the imprint.

The disadvantage of the known method, in particular in the case of the production of
25 solar cells in which the highly doped regions are arranged in a pattern of a series of parallel tracks or fingers, is that the diffusion between the tracks having a high concentration is highly sensitive to the atmosphere in the diffusion furnace, as a result of which the diffusion method is insufficiently stable as a production process. Furthermore the ratio between the high and low doping is dependent and therefore local doping cannot be
30 adjusted to the optimum. To obtain good contact with the metalisation placed on the highly doped regions, which metalisation is frequently applied by screen printing, a low surface resistance, and thus as high as possible a doping, is desired. For the regions located between the metalisation an increase in yield is possible, for example in the case of n-p-

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type solar cells, by passivation of the surface with thermal SiO_2 or PECVD SiN , as a result of which recombination of charge carriers at the surface is counteracted. This increase in yield can be achieved only if the doping is low.

One aim of the present invention is therefore to provide a method for making a semiconductor device, in particular a solar cell, with which regions of high and low doping can be applied efficiently in accurately determined positions on the substrate. A further aim of the invention is to provide a method with which the concentrations of the doping material in the regions of high and low doping can be adjusted relatively independently of one another.

To this end the method according to the invention is characterised in that before the diffusion step a diffusion barrier material is applied to the substrate at the location of the regions of low doping by imprinting with the barrier material in the pattern of the regions of low doping.

During the diffusion step, which usually will be carried out at temperatures of approximately 900°C , the substrate regions located beneath the barrier material are shielded by the latter from the diffusion material applied to the neighbouring regions. As a result the concentration in the regions of low doping can be freely adjusted accurately and independently of the concentration in the highly doped regions. Furthermore, with the method according to the invention a single screen printing step and a single drying step can suffice.

It is possible first to apply the doping material to the substrate as a uniform layer, for example by spraying, and then to print the barrier material by means of a printing technique onto the regions of the substrate with low doping, after which the diffusion step is carried out. In this embodiment the barrier material can delay the diffusion of the underlying diffusion material or it can have etching properties, so that the underlying diffusion during the diffusion step is etched out of the substrate. A barrier material which has etching properties is, for example, ZnO .

Alternatively, according to the invention the barrier material is first applied by screen printing, stencil printing, offset printing or tampon printing or using other printing techniques known per se to those regions of the substrate which are to have low doping. The doping material can then be applied as a single layer by spraying, spinning, immersing, vapour deposition or from the gas phase (such as, for example, by means of POCl_3 gas in a crystal tube) on top of the substrate and on top of the barrier material.

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Although this is not to be preferred from the production standpoint, the doping material can also be printed selectively onto the regions of the substrate for high doping, before or after applying the barrier material. The barrier material is, for example, a dielectric material such as Si_3N_4 , SiO_2 or TiO_2 , to which an n-type doping material, such as phosphorus (P), arsenic (As), antimony (Sb) or bismuth (Bi) can have been added, or a p-type doping material such as boron (B), aluminium (Al), gallium (Ga), indium (In) or thallium (Th). This material is printed onto the substrate in paste form and then sintered at temperatures between 200 °C and 1000 °C.

Following the diffusion step the surface resistance in the highly doped regions is, for example, between 10 and 60 ohm square, for a concentration of doping atoms of between 10^{16} cm^{-3} and 10^{21} cm^{-3} , for a diffusion depth beneath the substrate surface of between 0.1 μm and 0.5 μm . The surface resistance of the regions with low doping is between 40 ohm and 500 ohm square, for a concentration of doping atoms of between 10^{17} cm^{-3} and 10^{21} cm^{-3} , for a diffusion depth of between 0.1 μm and 0.5 μm .

A few embodiments of the method according to the present invention will be explained in more detail by way of example with reference to the appended diagrammatic drawing. In the drawing:

Fig. 1 shows a diagrammatic representation of a method according to the prior art,

Figs 2a, 2b and 2c show a first embodiment of a method according to the present invention using a uniform layer of doping material,

Figs 3a, 3b and 3c show an alternative embodiment of a method according to the invention with selective application of the doping material,

Figs 4a, 4b and 4c show an embodiment of the method according to the invention where the barrier material has etching properties and

Fig. 5 shows a concentration profile of a semiconductor device produced according to the invention.

Fig. 1 shows a p-type substrate consisting of, for example, silicon doped with n-type atoms. A doping material in the form of a paste, such as a phosphorus paste, is applied by means of screen printing to the substrate 1 above those regions of the substrate 1 which are to have high doping. Following a diffusion step at approximately 900 °C in a diffusion furnace there are highly doped regions 3 and regions 4, 4' of low doping, formed by lateral diffusion from the phosphorus paste 2 via the atmosphere in the diffusion furnace, in substrate 1.

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etching agent such as, for example, ZnO. During the diffusion step, which is carried out in Fig. 4b, the etching agent from the barrier material will etch away the diffusion regions located beneath this, so that the highly doped regions 6, 6' remain in the substrate in positions where the barrier material 5 - 5'' is absent. Metal contacts 8, 8' can then be
5 applied above the highly doped diffusion regions 6, 6', as shown in Fig. 4c.

This method has the advantage that an optical difference which can be used when aligning the metalisation pattern is produced between the positions of the barrier material and neighbouring locations. Furthermore, reduced reflection can be obtained with the construction according to Fig. 4c.

10 It is pointed out that although the method has been described with reference to a p-type substrate and an n-type doping material the method is also suitable for use with n-type substrates with p-type doping material.

Finally, Fig. 5 shows a plot of the concentration against the depth below the substrate surface for a semiconductor device produced in accordance with the present invention. The
15 process conditions for the production of the semiconductor device having the concentration profile according to Fig. 5 were as follows:

The barrier layer was applied from a print paste which was sintered in air at approximately 400 °C. This leads to a layer of approximately 1 µm thick SiO₂ of low porosity (> 80% volume of SiO₂). It is important that the paste shows few cracks in order
20 to achieve a maximum gain in efficiency. Partial coverage of the wafer with a barrier layer leads to a lower efficiency but not to short-circuiting of the cell, as is the case when a selective emitter is made with the aid of a resist to protect the locations where a highly doped emitter is needed.

After applying the barrier layer, a phosphorus-containing layer was applied by spin
25 coating using a phosphorus source in the liquid phase. Diffusion into the wafer was then carried at 900 °C for 10 minutes, which led to the pattern below the barrier layer as is indicated in Fig. 5.

To make cells, silver lines with a width of approximately 100 µm are then printed within the area previously etched by the barrier layer. The size of this etched area has been
30 chosen to be relatively large to prevent the risk of short-circuiting with the regions of low doping. This etched area is at least 150 µm wide. It can be seen from Fig. 5 that the concentration of donor atoms in the highly doped regions 6, 6' is appreciably higher and extends over a greater depth than the concentrations of doping material in regions below

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the barrier material 5 - 5". The low donor concentrations at the surface, as are shown in Fig. 5, are outstandingly suitable for surface passivation. This can lead to a significant rise in efficiency of the order of 5%, relative.

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6. Method according to one of the preceding claims, characterized in that the surface resistance of the highly doped regions is between 10 and 60 ohm square and the surface resistance of the regions of low doping is between 30 and 500 ohm square.

7. Method according to Claim 6, characterized in that the concentration of the doping material in the highly doped regions is between 10^{18} cm^{-3} and 10^{21} cm^{-3} , whilst the diffusion depth is between 0.1 μm and 0.5 μm , and in that the concentration of the doping material in the regions of low doping is between 10^{17} cm^{-3} and 10^{21} cm^{-3} for a diffusion depth of between 0.1 μm and 0.5 μm .

8. Method according to one of the preceding claims, characterized in that an etching material is added to the diffusion material (5, 5', 5'') to etch away the substrate.

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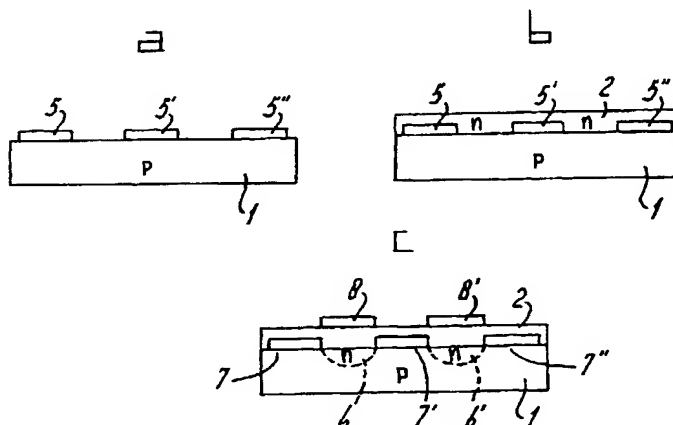
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Alkmaar (NL).

For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.

(54) Title: **METHOD FOR THE PRODUCTION OF A SEMICONDUCTOR DEVICE**



(57) Abstract: The invention relates to a method for making a semiconductor device having a pattern of highly doped regions (6, 6') located some distance apart in a semiconductor substrate (1) and regions (7, 7', 7'') of low doping located between the highly doped regions (6, 6'). According to the invention a diffusion barrier material (5, 5', 5'') is applied to the semiconductor substrate at the location of the regions of low doping by means of imprinting with the barrier material in the pattern of the regions of low doping. The doping material is applied after or before imprinting with the barrier material so that the highly doped regions are formed essentially between the barrier material in the substrate. With the method according to the invention the doping concentrations in the regions of low doping and in the highly doped regions can be freely adjusted independently of one another so that a relatively low surface resistance can be obtained for the highly doped regions to give good conducting contact with the metalisation and a high surface resistance can be achieved in the regions of low doping.

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fig-1

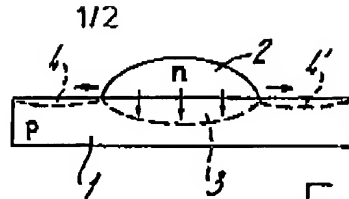


fig-2a

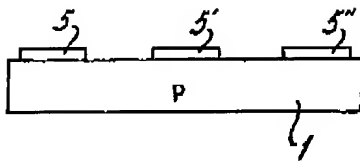


fig-2b

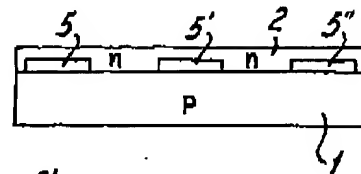


fig-2c

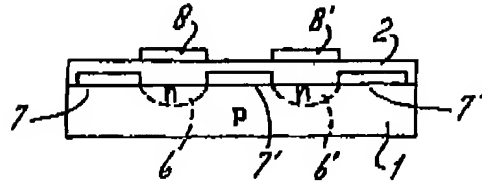


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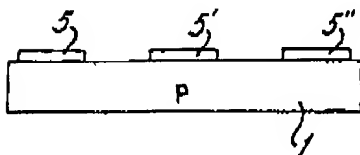


fig-3b

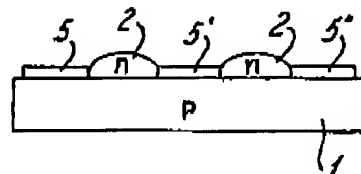


fig-3c

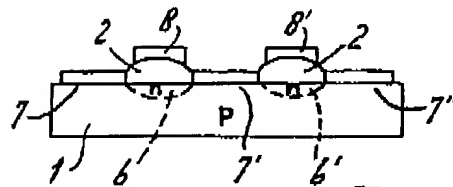


fig-4a

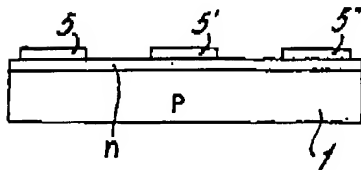


fig-4b

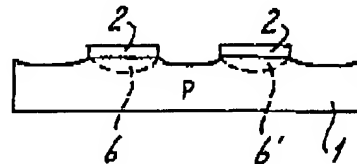


fig-4c



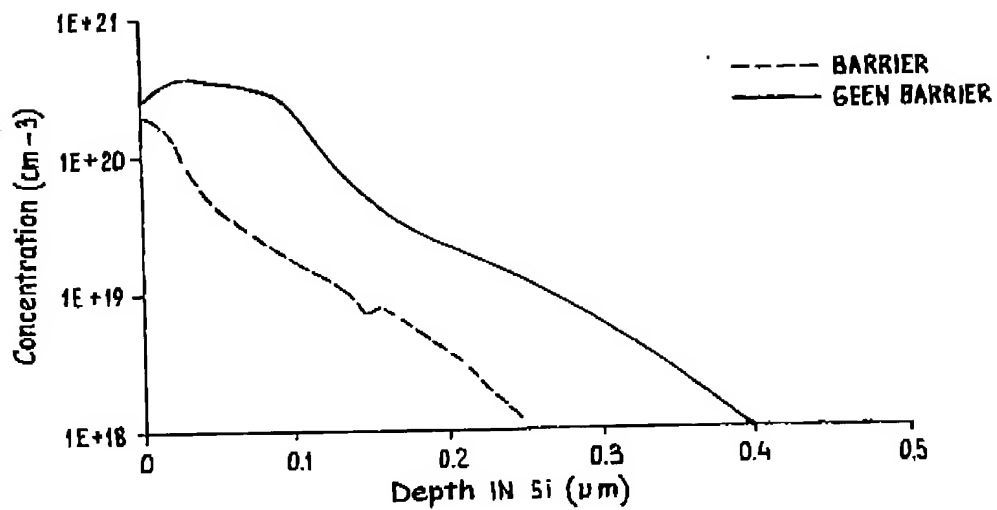
SUBSTITUTE SHEET (RULE 26)

WO 01/24279

PCT/NL00/00613

2/2

fig-5



SUBSTITUTE SHEET (RULE 26)

COMBINED DECLARATION AND POWER OF ATTORNEY

(ORIGINAL DESIGN, NATIONAL STAGE OF PCT OR CIP APPLICATION)

As a below named inventor, I hereby declare that

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Method for the production of a semiconductor device

the specification of which: (complete (a), (b) or (c) for type of application)

REGULAR OR DESIGN APPLICATION

- a. ☐ is attached hereto.
b. ☐ was filed on _____ as Application
Serial No. _____ and was amended on _____
(if applicable)

PCT FILED APPLICATION ENTERING NATIONAL STAGE

- c. ☒ was described and claimed in International application No. PCT/NL00/00613
filed on 1 September 2000
and as amended on _____ (if any)

ACKNOWLEDGEMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, paragraph 1.56(a).

In compliance with this duty there is attached an information
disclosure statement 37 CFR 1.97

PRIORITY CLAIM

I hereby claim foreign priority benefits under Title 35, United States Code paragraph 119 of any foreign application (s) for patent of inventor's certificate listed below and have also identified below any foreign application for patent of inventor's certificate having a filing date before that of the application on which priority is claimed.

(complete (d) or (e))

- d. ☐ no such applications have been filed
e. ☒ such applications have been filed as follows

**EARLIEST FOREIGN APPLICATION(S), IF ANY FILED WITHIN 12 MONTHS
(6 MONTHS FOR DESIGN) PRIOR TO SAID APPLICATION**

Country	Application Number	Date of filing (day, month, year)	Date of Issue (day, month, year)	Priority claimed
The Netherlands	1012961	2 September 1999		Yes

**ALL FOREIGN APPLICATION(S), IF ANY FILED MORE THAN 12 MONTHS
(6 MONTHS FOR DESIGN) PRIOR TO SAID APPLICATION**

CONTINUATION-IN-PART

(Complete this part only if this is a continuation-in-part application)

I hereby declare claim the benefit under Title 35, United States code, paragraph 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claim of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, paragraph 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, paragraph 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) (Filing date) (Status) (patented, pending, abandoned)

(Application Serial No.) (Filing date) (Status) (patented, pending, abandoned)

POWER OF ATTORNEY

As a named inventor, I hereby appoint the following attorney(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Robert J. PATCH, Reg. No. 17,355, Andrew J. PATCH, Reg. No. 32,925, Robert F. HARGEST, Reg. No. 25,590, Benoît CASTEL, Reg. No. 35,041, Eric Jensen, Reg. No. 37,855, and Thomas W. PERKINS, Reg. No. 33,027 and Roland E. Long, Jr. Reg. No. 41,949 c/o YOUNG & THOMPSON, Second Floor, 745 South 23rd Street, Arlington, Virginia 22202.

Address all telephone calls to Young & Thompson at 703/521-2297.

I hereby declare that all statements made herein of my own knowledge, are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that wilful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code and that such wilful false statements may jeopardize the validity of the application or any patent issued thereon.

100 Full name of sole or first inventor: **BULTMAN, Jan Hendrik**

Inventor's signature



Date 20 June 2002

Country of Citizenship: The Netherlands

Residence: ALKMAAR, The Netherlands **NLX**

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